Docket No.: 021404-0012US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Nicholas J. Witchey

Application No.: 10/712,084 Confirmation No.: 7909

Filed: November 13, 2003 Art Unit: 2451

For: Communication Protocol Converter and Method of Protocol Conversion Examiner: K. Q. Dinh

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on August 20, 2010, and is in furtherance of said Notice of Appeal.

The fees required under §41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. §41.37 and M.P.E.P. § 1205.2:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Nicholas J. Witchey

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 11 claims pending in application.

B. Current Status of Claims

1. Claims canceled: None
2. Claims withdrawn from consideration but not canceled: 12-14
3. Claims pending: 1-11
4. Claims rejected: 1-11

C. Claims On Appeal

The claims on appeal are claims 1-11

IV. STATUS OF AMENDMENTS

Applicant filed an Amendment After Final Rejection on July 26, 2010. The Examiner responded to the Amendment After Final Rejection in an Advisory Action mailed August 12, 2010. In the Advisory Action, the Examiner indicated that Applicants' proposed amendments to Claims 1-11 would not be entered.

Accordingly, the claims enclosed herein as Appendix A do not incorporate either the amendments to Claims 1-11, as indicated in the paper filed. However, the claims in Appendix A do incorporate the amendments indicated in the paper filed by Applicant on July 26, 2010.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention generally relates to a communication protocol converter to allow a legacy device utilizing IPv4 to operate across the network using IPv6. In a first embodiment of the invention, two modular Ethernet connectors are placed side-by-side. A first modular connector receives IPv4 Ethernet data which is converted to a raw data signal. The data is transmitted from the first modular connector to a second modular connector by a bidirectional data line. The second connector receives the raw data, and a raw data-to-Ethernet conversion is completed providing output at IPv6. The present invention utilizes the form factor structure of the Ethernet connectors, so that the entire electronic circuitry is contained within the connectors to complete the conversion. An alternate embodiment incorporates the connectors into a single housing and the conversion is completed internally by a microprocessor and embedded software. A method of IPv4 to IPv6 conversion is additionally disclosed.

Claim 1 specifies: A communication protocol converter comprising:

(a) a first modular communication jack having:

i) a housing defining an open cavity and a segregated interior chamber;

ii) a connector port having a plurality of electrical contacts positioned within said open cavity;

iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port wherein the circuitry components are positioned on both sides of the at least one circuit board; and

iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data whereby the memory is interconnected to a bi-directional data line that allows the input and output of raw data;

(b) a second modular communication jack having:

i) a housing defining an open cavity and a segregated interior chamber;

ii) a connector port having a plurality of electrical contacts positioned within said open cavity;

iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port;

iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for said second communication protocol for receiving converted data wherein the memory is interconnected with the bi-directional line to receive input of raw data from the first modular communication jack and further wherein said memory stores data utilized by a controller block;

v) the controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics wherein said controller block communicates with Ethernet through Ethernet interface; and

(c) a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack.

Support for this claim language can be found in the originally filed specification on page 1, Paragraph 3; Page 2-3, Paragraph 7, Page 3, Paragraph 8 and 9; Page 5, Paragraph 23 and 24.

Claim 7 specifies: A communication protocol converter comprising:

a housing defining first and second open cavities and a segregated interior chamber;

each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a second communication protocol;

at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bidirectionally translates communication protocols wherein the housing allows for the at least one circuit board to electronically communicate with both the first connector port and the second connector port; and

a microprocessor employing embedded software that receives Internet protocol 4 Ethernet data; removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data, the embedded software located on flash memory which is utilized by the microprocessor to perform its functions.

Support for this claim language can be found in the originally filed specification on Page 3, Paragraph 4 and Page 4, Paragraph 11.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-11 under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510).

VII. ARGUMENT

On **November 13, 2003**, the Appellant filed Application Number 10/712,084 for Communication Protocol Converter and Method of Protocol Conversion.

On **October 6, 2008**, the Patent Office sent a Office Action with a restriction requirement on Claims 1-14.

On **November 6, 2008**, the Appellant responded to the Office Action by filing a response and electing Claims 1-11.

On **December 11, 2008**, the Patent Office sent a notice of Non-Final Office Action rejecting Claims 1-11. Claims 1-11 were rejected under 35 U.S.C. §102(e) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681).

On **March 11, 2009**, the Appellant responded to the Office Action by filing an Amendment.

On **June 8, 2009**, the Patent Office sent a notice of Final Office Action rejecting Claims 1-11. Claims 1-11 were rejected under 35 U.S.C. §102(e) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681).

On **August 10, 2009**, the Appellant responded to the Office Action by filing an Amendment.

On **August 19, 2009**, the Patent Office sent a notice of Advisory Action.

On **August 21, 2009**, the Patent Office sent a Office Communication regarding an Interview Summary.

On **September 2, 2009**, the Appellant responded to the Advisory Action by filing a Request for Continued Examination.

On **September 2, 2009**, the Appellant responded to an Interview Summary.

On **October 2, 2009**, the Patent Office sent a Non-Final Office Action rejecting Claims 1-11. Claims 1-11 were rejected under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510).

On **February 1, 2010**, the Appellant responded to the Office Action by filing an Amendment.

On **May 25, 2010**, the Patent Office sent a Final Office Action rejecting Claims 1-11. Claims 1-11 were rejected under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510).

On **July 26, 2010**, the Appellant responds to the Office Action by filing an Amendment.

On **August 12, 2010**, the Patent Office sent a notice of Advisory Action.

On **August 20, 2010**, the Appellant responds to the Office Action by filing a Notice of Appeal.

1. **Claims 1-11 were rejected under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510).**

The Patent Office has rejected Claims 1-11 under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510) alleging that Claim 1, *Hovell et al.* discloses a communication protocol converter comprising: (a) a first modular communication jack having: a housing defining an open cavity and a segregated interior chamber, a connector port having a plurality of electrical contacts positioned within said open cavity, at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; wherein the circuitry components are positioned on both sides of the at least one circuit board (ports connecting 62(A, B) and 72(A, B) of fig. 2, see fig. 2, col.8 line 10 to col.9 line 20); and iv) a memory positioned on said circuit

board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to col.7 line 50); whereby the memory is interconnected to a bi-directional data line that allows the input and output of raw data (writing and accessing data from/to the storage (68A fig. 2), see col.8 line 10 to col.9 line 20) (b) a second modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; a memory positioned on said circuit board in electrical communication with said conversion circuitry for said second communication protocol for receiving converted data (see fig. 2, col.7 line 17 to col.8 line 58) wherein the memory is connected with the bi-directional line to receive input of raw data from the first modular communication jack; and (c) a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack (processing data in/out of the storage, see col.8 lines 10-58).

Hovell et al. discloses a tunnel is established across an IPv4 domain for the transport of packets from a source host on one IPv6 domain to a destination host on another IPv6 domain, there being respective interfaces between the IPv4 domain and the IPv6 domains.

Hies et al. discloses a method for providing handling of data sent between a first network and at least a second network and a third network, wherein the first network is of a first protocol and the at least second and third networks are of a second protocol at least partially overlap is provided. A packet transmitted from the first network is received. The packet has a first address prefix if the packet is directed to the second network and has a second address prefix if the packet is directed to the third network. A destination address of the packet and a source address of the packet are translated from the first protocol to the second protocol. The packet is directed to the second network if the packet has the first address prefix. The packet is directed to the third network if the packet has the second address prefix.

The Office Action admits, however, that *Hovell et al.* does not specifically disclose a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics and the memory for storing data utilized by a controller block and to communicate with Ethernet through Ethernet interface. However, the Office Action alleges that *Hies et al.* discloses a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics and the memory for storing data utilized by a controller block (memory block 65 fig. 6) and to communicate with Ethernet through Ethernet interface for storing data that utilized by a controller block (memory block 65 fig. 6) (using a CPU to control routing table computations and performing protocol conversions from IPV4 to IPV6 and a memory block to control the operating system or applications using Ethernet interfaces, see fig. 6, co1.6 line 24 to col.7 line 58). The Patent Office states it would have been obvious to one of the ordinary skill in the art at the time the invention was made to implement *Hies et al.* teachings into the *Hovell et al.'s* converter to process data information because it would have allowed the master processor to efficiently perform routing computations, network diagnostics in a communication network (see *Hies'* co1.7 lines 2-23).

The Patent Office alleges that as to Claim 7, *Hovell et al.* discloses a communication protocol converter comprising: a housing defining first and second open cavities and a segregated interior chamber; each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a second communication protocol (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to co1.7 line 50); and at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bi-directionally translates communication

protocols (network protocol translation, see fig. 2, col.7 line 17 to col.8 line 58), wherein the housing allows for the at least one circuit board to electronically communicate with both the first connector port and the second connector port and a microprocessor employing embedded software that converts Ethernet data from internet protocol version 4 to internet protocol version 6 (converting data from IPV4 to IPV6, see fig. 2, col.7 line 17 to col.8 line 58).

The Patent Office alleges that *Hovell et al.* does not specifically disclose a microprocessor to receive Internet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data and a embedded software located on flash memory which is utilized by the micropressor to perform its functions. However, the Office Action alleges that *Hies et al.* discloses a microprocessor receive Internet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data and a embedded software located on flash memory which is utilized by the microprocessor to perform its functions (memory block 65 fig. 6) (using a CPU to control routing table computations and performing protocol conversions from IPV4 to IPV6 and a memory block to control the operating system or applications, see fig. 6, col.6 line 24 to col.7 line 58). The Patent Office alleges it would have been obvious to one of the ordinary skill in the art at the time the invention was made to implement *Hies et al.'s* teachings into the *Hovell et al.'s* converter to process data information because it would have allowed the master processor to efficiently perform routing computations, network diagnostics in a communication network (see *Hies et al.'s* col.7 lines 2-23).

With respect to independent Claim 1, the Office Action alleges that *Hies et al.* teaches "a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals" as recited in Claim 1. (Office Action, p. 4, emphasis added.) As illustrated in fig. 6 of *Hies et al.*, processor 63 clearly does not "handle[s] all the conversion between raw data and Ethernet, including . . . analog signals" because processor 63 is connected to interface 68 over bus 15. *Hies et al.* fails to provide any further details on how the processor converts data in its specification, any analog signals received at interface 68 would have to be converted to digital signals and then read or written to the processor 63 over bus 15.

Applicant notes that bus 15 of *Hies et al.* can be a digital bus such as a PCI bus. Even if another type of bus was used, nothing in *Hies et al.* teaches or even suggests that the bus used can connect analog signals to processor 63.

With respect to independent Claim 7, the Office Action alleges that *Hies et al.* "discloses a microprocessor receive Internet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data." (Office Action, p. 6.) Nothing in *Hies et al.* teaches or suggests the processor "handles all the conversion between raw data and Ethernet, including processing of digital and analog signals" as recited in Claim 7. As discussed above, *Hies et al.*, processor 63 clearly does not process analog signals because processor 63 is connected to interface 68 over bus 15. In other words, the prior art references require additional structural elements or processes in order to perform the communication protocol conversion taught in the present invention.

Additionally, the Office Action alleges that *Hies et al.* teaches "embedded software located on flash memory which is utilized by the microprocessor to perform its function (memory block 65 fig. 6)." (Office Action, p. 6.) Nothing in *Hies et al.* teaches or suggests that the memory is flash memory.

It is further submitted that the question under §103 is whether the totality of the art would collectively suggest the claimed invention to one of ordinary skill in this art. *In re Simon*, 461 F.2d 1387, 174 USPQ 114 (CCPA 1972).

That elements, even distinguishing elements, are disclosed in the art is alone insufficient. It is common to find elements somewhere in the art. Moreover, most if not all elements perform their ordained and expected functions. The test is whether the invention as a whole, in light of the teaching of the reference, would have been obvious to one of ordinary skill in the art at the time the invention was made. *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983).

It is insufficient that the art disclosed component's of Applicants' invention. A teaching, suggestion, or incentive must exit to make the combination made by Applicants. *Interconnect Planning Corp. v. Feil,* 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1988).

As set forth in MPEP § 2143(A), "[t]he rationale to support a conclusion that the claim would have been obvious is that all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination yielded nothing more than predictable results to one of ordinary skill in the art." (underlining added for emphasis). MPEP § 2143(A), p. 2100-129, Eighth Edition, Rev. 6, Sept. 2007. Further, as set forth in MPEP § 2143.01, under *KSR*, " [i]f the proposed modification or combination of prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." MPEP § 2143.01, p. 2100-141, Eighth Edition, Rev. 6, Sept. 2007.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Applicant on July 26, 2010.

Applicant believes a fee is due with the filing of this Appeal Brief, we hereby authorize the Commissioner to hereby charge Deposit Account No. 50-2191.

Dated: October 20, 2010

Respectfully submitted,

By_____

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/712,084

1. (Previously Presented) A communication protocol converter comprising:

(a) a first modular communication jack having:

i) a housing defining an open cavity and a segregated interior chamber;

ii) a connector port having a plurality of electrical contacts positioned within said open cavity;

iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port wherein the circuitry components are positioned on both sides of the at least one circuit board; and

iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data whereby the memory is interconnected to a bi-directional data line that allows the input and output of raw data;

(b) a second modular communication jack having:

i) a housing defining an open cavity and a segregated interior chamber;

ii) a connector port having a plurality of electrical contacts positioned within said open cavity;

iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port;

iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for said second communication protocol for receiving converted data wherein the memory is interconnected with the bi-directional line to receive input of raw data from the first modular communication jack and further wherein said memory stores data utilized by a controller block;

v) the controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as

well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics wherein said controller block communicates with Ethernet through Ethernet interface; and

(c) a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack.

2. (Original) The communication protocol converter of claim 1 wherein said first communication protocol is Internet protocol version 4 and said second communication protocol is Internet protocol version 6.

3. (Original) The communication protocol converter of claim 1 wherein said first communication protocol is Internet protocol version 6 and said second communication protocol is Internet protocol version 4.

4. (Original) The communication protocol converter of claim 1 wherein said conversion circuitry components of said first and second modular communications jacks includes magnetic circuitry and controller circuitry.

5. (Original) The communication protocol converter of claim 4 wherein said conversion circuitry components includes LED circuitry.

6. (Original) The communication protocol converter of claim 4 wherein said circuit boards each define first and second opposed sides and said conversion circuitry components are positioned on both first and second sides of said circuit boards.

7. (Previously Presented) A communication protocol converter comprising:

a housing defining first and second open cavities and a segregated interior chamber;

each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a second communication protocol;

at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bidirectionally

translates communication protocols wherein the housing allows for the at least one circuit board to electronically communicate with both the first connector port and the second connector port; and

a microprocessor employing embedded software that receives Internet protocol 4 Ethernet data; removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data, the embedded software located on flash memory which is utilized by the microprocessor to perform its functions.

8. (Original) The communication protocol converter of claim 7 wherein said protocol conversion circuitry comprises; a microprocessor incorporating embedded software for converting a first communication protocol received at said first connector port to a second communication protocol output to said second connector port.

9. (Original) The communication protocol converter of claim 8 wherein said microprocessor converts a second communication received at said second connector port to a first communication protocol output to said first connector port.

10. (Original) The communication protocol converter of claim 7 wherein said first communication protocol is Internet protocol version 4 and said second communication protocol is Internet protocol version 6.

11. (Original) The communication protocol converter of claim 7 wherein said first communication protocol is Internet protocol version 6 and said second communication protocol is Internet protocol version 4.

12. (Withdrawn) A method of converting Ethernet data from a Internet protocol 4 to Internet protocol 6 comprising the steps of: (a) receiving Internet protocol 4 Ethernet data; (b) removing Internet protocol 4 header data; (c) inserting Internet protocol 6 header data; (d) recalculating necessary Internet protocol header fields; (e) outputting corresponding Internet protocol 6 Ethernet data.

13. (Withdrawn) A method of converting Ethernet data from a Internet protocol 6 to Internet protocol 4 comprising the steps of: (a) receiving Internet protocol 6 Ethernet data; (b) removing

Internet protocol 6 header data; (c) inserting Internet protocol 4 header data; (d) recalculating necessary Internet Protocol header fields and IPv4 checksum (e) outputting corresponding Internet protocol 4 Ethernet data.

14. (Withdrawn) A method of converting Ethernet data from a first communication protocol to a second communication protocol comprising the steps of: (a) receiving Ethernet data having a first communication protocol; (b) removing the first communication protocol header data; (c) inserting a second communication protocol header data; (d) recalculating any necessary protocol header fields and options; (e) outputting corresponding Ethernet data having a second communication protocol.

APPENDIX B

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.